CLAIMS

1. A receiver comprising:

a plurality of receiver branches operable to receive signals;

a plurality of sample-and-hold circuits, each of which is connected to corresponding one of said plurality of receiver branches, each of said plurality of sample-and-hold circuits being operable to extract a discrete value from an output signal from corresponding one of said plurality of receiver branches;

a switch connected to said plurality of sample-and-hold circuits, said switch being operable to allow output signals from said plurality of sample-and-hold circuits to be selectively fed out of said switch at time intervals; and

a demodulating unit connected to said switch, said demodulating unit being operable to demodulate data from output signals from said switch.

2. A receiver as defined in claim 1, wherein each of said receiver branches includes a band pass filter operable to allow corresponding one of the signals to travel through a certain band, and a first amplifier operable to amplify an output signal from said band pass filter.

3. A receiver as defined in claim 2, wherein each of said receiver branches includes an antenna.

4. A receiver as defined in claim 1, further comprising:

an analog-to-digital converter connected between said switch and said demodulating unit, said analog-to-digital converter being operable to convert the output signals from said switch in value from analog values to digital values.

5. A receiver as defined in claim 4, further comprising:

a clock-generating unit operable to generate clock signals to be fed into said plurality of sample-and-hold circuits, said switch, and said analog-to-digital converter.

6. A receiver as defined in claim 5, further comprising:

an amplifier connected to said clock-generating unit, said amplifier being operable to amplify the clock signals from said clock-generating unit by an integer multiple comparable in number to said plurality of receiver branches,

wherein an output from said amplifier is fed into said switch and said analog-to-digital converter.

7. A receiver as defined in claim 4, further comprising:

a second amplifier connected to said analog-to-digital converter at an input of said analog-to-digital converter;

a gain control unit operable to control a gain in said second amplifier; and

a gain control information-detecting unit operable to detect gain control information to be fed into said gain control unit.

8. A receiver as defined in claim 7, wherein said gain control information is a signal-to-noise ratio (hereinafter called an "S/N ratio") detected by said demodulating unit.

9. A receiver as defined in claim 7, wherein said gain control information is a bit error rate (hereinafter called a "BER") detected by said demodulating unit.

10. A receiver as defined in claim 7, wherein said second amplifier has an amplification degree within a dynamic range of said analog-to-digital converter.

11. A receiver as defined in claim 4, further comprising:

a plurality of third amplifiers, each of which is connected to corresponding one of said plurality of sample-and-hold circuits, each of said plurality of third amplifiers being operable to amplify an output from corresponding one of said plurality of sample-and-hold circuits;

a gain control unit operable to control gains in said plurality of third amplifiers; and

a gain control information-detecting unit operable to detect gain control information to be fed into said gain control unit.

12. A receiver as defined in claim 11, wherein each of said plurality of third amplifiers has a substantially identical gain characteristic.

13. A receiver as defined in claim 12, wherein each of said plurality of third amplifiers has an amplification degree, whereby a highest gain possessed by one of output signals from said plurality of sample-and-hold circuits to be amplified by said plurality of third amplifiers falls within a dynamic range of said analog-to-digital converter.

14. A receiver as defined in claim 5, further comprising:

a clock control unit operable to control a clock frequency in said clock-generating unit.

15. A receiver as defined in claim 14, wherein said clock control unit is operable to divide the clock frequency in said clock-generating unit in accordance with a number of frequency division multiplex signals in operative use when the signals received by said plurality of receiver branches include the frequency division multiplex signals.

16. A receiver as defined in claim 1, wherein a length of wiring extending from an input end of each of said plurality of receiver branches to each of said sample-and-hold circuits is substantially identical for each of said plurality of receiver branches.

17. A receiver as defined in claim 1, wherein a load of wiring extending from an input end of each of said plurality of receiver branches to each of said sample-and-hold circuits is substantially identical for each of said plurality of receiver branches.

18. A receiver comprising:

a plurality of receiver branches operable to receive signals;

a switch connected to said plurality of receiver branches, said switch being operable to allow output signals from said plurality of receiver branches to be

selectively fed out of said switch at time intervals;

a sample-and-hold circuit connected to said switch, said sample-and-hold circuit being operable to extract discrete values from output signals from said switch;

a variable amplifier connected to said sample-and-hold circuit, said variable amplifier being operable to amplify output signals from said sample-and-hold circuit;

a gain control unit operable to control a gain in said variable amplifier;

a gain control information-detecting unit operable to detect gain control information to be fed into said gain control unit;

an analog-to-digital converter connected to said variable amplifier, said analog-to-digital converter being operable to convert output signals from said variable amplifier in value from analog values to digital values; and

a demodulating unit connected to said analog-to-digital converter, said demodulating unit being operable to demodulate data from output signals from said analog-to-digital converter,

wherein said gain control unit executes control such that the output signals from said variable amplifier fall within a dynamic range of said analog-to-digital converter.

19. A receiver comprising:

a plurality of receiver branches operable to receive signals;

a switch connected to said plurality of receiver branches, said switch being operable to allow output signals from said plurality of receiver branches to be selectively fed out of said switch at time intervals;

a sample-and-hold circuit connected to said switch, said sample-and-hold circuit being operable to extract discrete values from output signals from said switch;

an analog-to-digital converter connected to said sample-and-hold circuit, said analog-to-digital converter being operable to convert output signals from said sample-and-hold circuit in value from analog values to digital values;

a demodulating unit connected to said analog-to-digital converter, said demodulating unit being operable to demodulate data from output signals from said analog-to-digital converter;

a clock-generating unit operable to generate clock signals to be fed into said switch, said sample-and-hold circuit, and said analog-to-digital converter; and

a clock control unit operable to control a clock frequency in said clock-generating unit.